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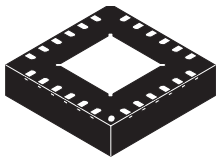
RoHS

Brushless DC 1.0 AMP 28 VOLT Motor Driver IC

34929

BRUSHLESS DC MOTOR DRIVER



QFN SUFFIX
98ARH99033A
24-PIN QFN (4X4X1)

The 34929 Brushless DC (BLDC) Motor Driver IC is a complete BLDC motor driver system in one chip. It is designed to efficiently drive three-phase BLDC motors up to 1A and 28V, and has built in protection features making it ideal for a variety of consumer, portable, and office applications containing small motors. It incorporates digital I/O, making it easy to use with an MCU in a closed-loop motor control system. It has a built-in Hall-effect sensors interface and a Hall sensors voltage supply, so it can operate BLDC motors as a stand-alone controller/driver. Its sophisticated analog/mixed-signal state machine accommodates several modes of operation, including: Forward (CW), Reverse (CCW), Run/Stop, Braking, Variable Speed (External PWM), and Torque Limit (maximum-current-limit) modes.

Features

- Single-Supply Operation (8V–28V)
- Built-in Hall Sensors Controlled-Supply (VH)
- 3-Phase Hall Sensors Interface
- Two Tachometer Outputs (1X and 3X Hall Frequency)
- Adjustable Maximum Current Limit (Torque Limiting)
- Adjustable Stalled Rotor Detection and Protection
- Short Circuit Detection and Protection
- Over-Temperature Detection and Thermal Shutdown
- Undervoltage Detection and Shutdown
- Pb-Free Packaging Designated by Suffix Code EP.

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC34929EP	-0°C to 85°C	24 QFN

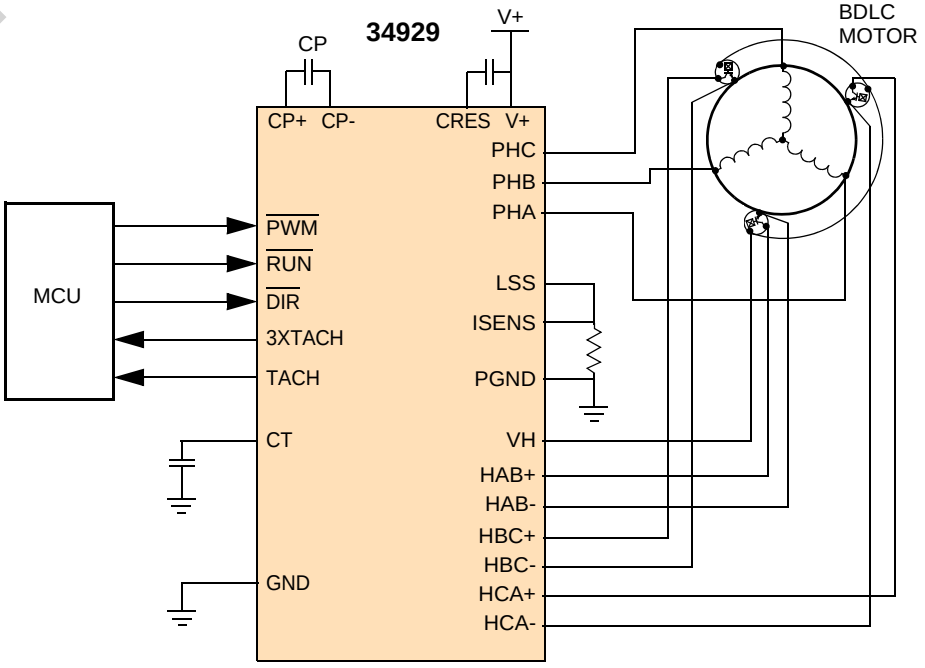


Figure 1. 34929 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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INTERNAL BLOCK DIAGRAM

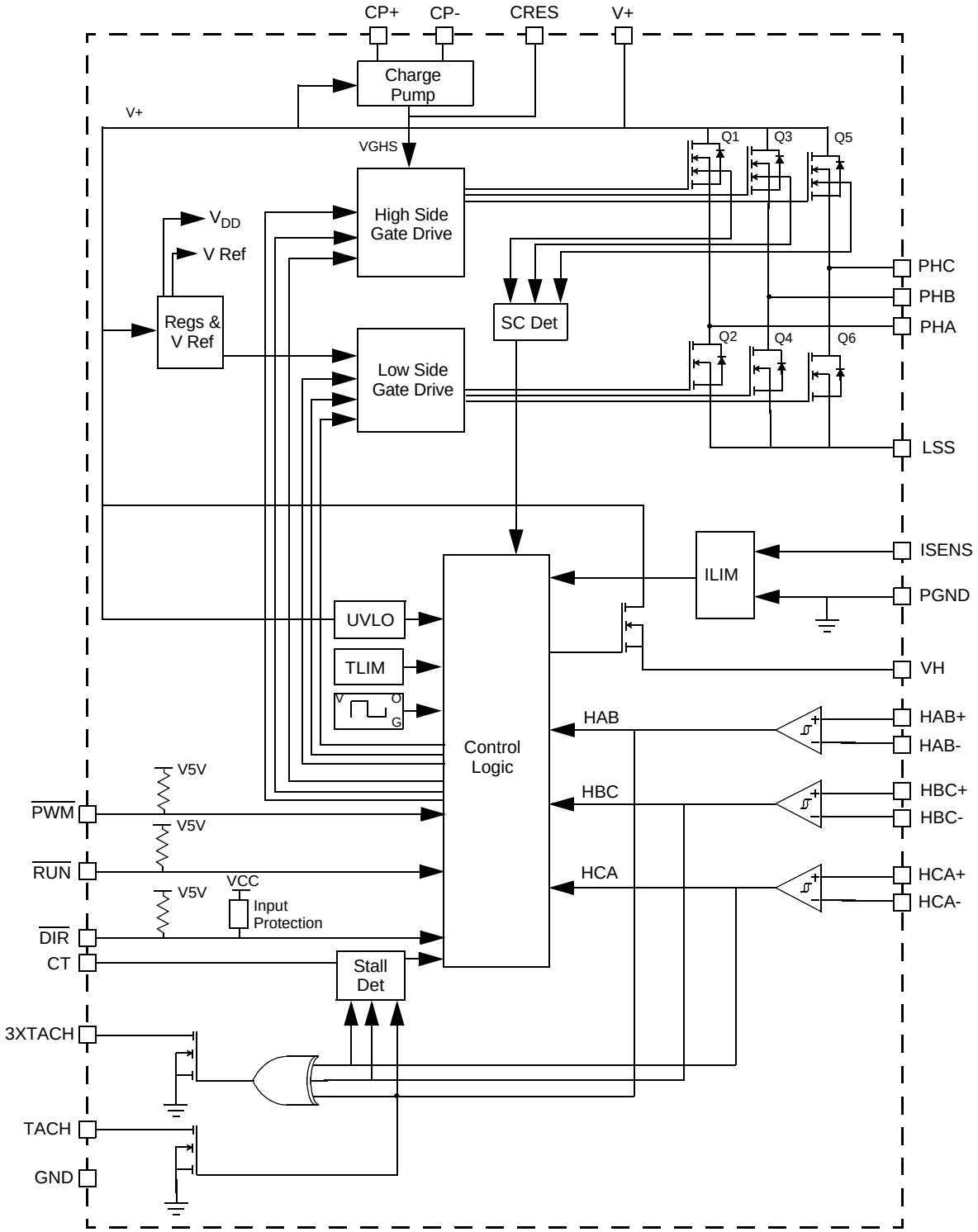


Figure 2. 34929 Simplified Internal Block Diagram

PIN CONNECTIONS

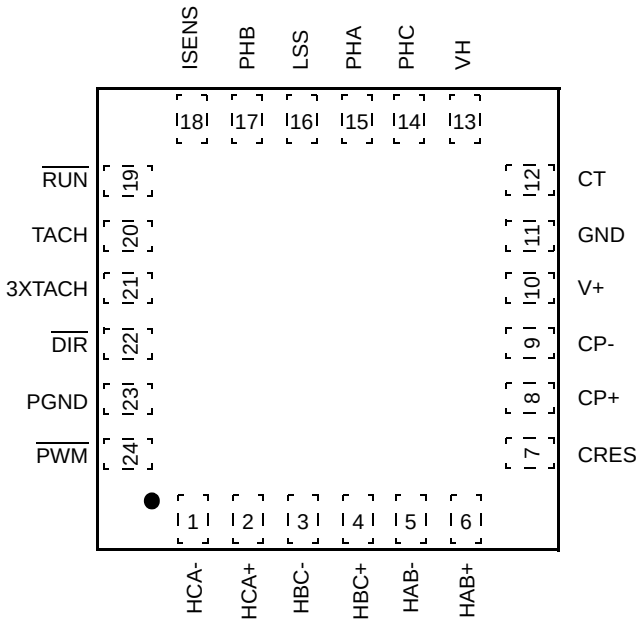


Figure 3. 34929 Pin Connections

Table 1. 34929 Pin Definitions

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	HCA-	INPUT	HALL CA NEG	RECEIVES NEGATIVE OUTPUT FROM SENSOR LOCATED BETWEEN ‘C’ AND ‘A’ PHASES
2	HCA+	INPUT	HALL CA POS	RECEIVES POSITIVE OUTPUT FROM SENSOR LOCATED BETWEEN ‘C’ AND ‘A’ PHASES
3	HBC-	INPUT	HALL BC NEG	RECEIVES NEGATIVE OUTPUT FROM SENSOR LOCATED BETWEEN ‘B’ AND ‘C’ PHASES
4	HBC+	INPUT	HALL BC POS	RECEIVES POSITIVE OUTPUT FROM SENSOR LOCATED BETWEEN ‘B’ AND ‘C’ PHASES
5	HAB-	INPUT	HALL AB NEG	RECEIVES NEGATIVE OUTPUT FROM SENSOR LOCATED BETWEEN ‘A’ AND ‘B’ PHASES
6	HAB+	INPUT	HALL AB POS	RECEIVES POSITIVE OUTPUT FROM SENSOR LOCATED BETWEEN ‘A’ AND ‘B’ PHASES
7	CRES	COMPONENT	RESERVOIR CAP	EXTERNAL CHARGE PUMP RESEVOIR CAP
8	CP+	COMPONENT	CHARGE PUMP POS	POSITIVE SIDE OF CHARGE PUMPING CAP
9	CP-	COMPONENT	CHARGE PUMP NEG	NEGATIVE SIDE OF CHARGE PUMPING CAP
10	V+	SUPPLY	POSITIVE SUPPLY	MAIN SUPPLY INPUT FOR DEVICE AND MOTOR
23	PGND	RETURN	POWER GROUND	POWER GROUND
12	CT	COMPONENT	TIMING CAP	EXTERNAL CAP FOR STALL DETECT TIMING
13	VH	OUTPUT	HALL VOLTAGE	SUPPLY VOLTAGE FOR THE EXTERNAL HALL SENSORS
14	PHC	OUTPUT	PHASE C OUTPUT	HALF BRIDGE OUTPUT FOR PHASE “C” MOTOR WINDING
15	PHA	OUTPUT	PHASE A OUTPUT	HALF BRIDGE OUTPUT FOR PHASE “A” MOTOR WINDING
16	LSS	RETURN	LOW SIDE SOURCES	COMMON SOURCE PIN FOR LOWER HALF OF BRIDGE
17	PHB	OUTPUT	PHASE B OUTPUT	HALF BRIDGE OUTPUT FOR PHASE “B” MOTOR WINDING

Table 1. 34929 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Formal Name	Definition
19	$\overline{\text{RUN}}$	INPUT	RUN	RUN/STOP CONTROL INPUT (ACTIVE LOW = MOTOR RUNNING)
20	TACH	OUTPUT	TACH OUTPUT	OPEN-DRAIN-BUFFERED OUTPUT OF SENSOR ‘AB’
21	3XTACH	OUTPUT	3X TACH OUTPUT	OPEN-DRAIN-BUFFERED, EXOR’ED OUTPUT OF ALL THREE SENSORS
22	$\overline{\text{DIR}}$	INPUT	DIRECTION	DIRECTION CONTROL INPUT (ACTIVE LOW = CW ROTATION)
11	GND	RETURN	SIGNAL GROUND	SIGNAL GROUND FOR DEVICE
24	$\overline{\text{PWM}}$	INPUT	PWM OR ENABLE	PWM SIGNAL INPUT (ACTIVE LOW = OUTPUTS ENABLED)
18	ISENS	INPUT	CURRENT SENSE	CURRENT LIMITING SENSE RESISTOR INPUT

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Transient Voltage	$V+_{TRANS}$	42	V
Signal I/O Pins	$V_{I/O}$	-0.6 to 5.5	V
Open Drain Outputs (TACH and 3XTACH)	$TACH_{OUT}$	42	V
Bridge Output Continuous Current	$I_{O(CONT)}$	1.0	A
Bridge Output Peak Current	$I_{O(PK)}$	1.5	A
Bridge Output Voltage	V_O	-1.0 to (V+) +1.0	V
Hall Voltage Supply Current	I_{VH}	30	mA
ESD Voltage (1) Human Body Model (HBM) Machine Model (MM)	V_{ESD}	 2000 200	V
THERMAL RATINGS			
Operating Ambient Temperature	T_A	-0 to 85	°C
Maximum Junction Temperature	T_{J-MAX}	150	°C
Storage Temperature	T_{STG}	-0 to 150	°C
THERMAL RESISTANCE			
Junction to Ambient (2)	$R_{\theta JA}$	<125	°C/W
Power Dissipation (3)	P_D	1.0	W
Peak Package Reflow Temperature During Reflow (4), (5)	T_{PPRT}	Note 5	°C

Notes

1. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0pF).
2. With PCB Layout comparable top copper and vias as shown in Figure 4, and bottom thermal ground plane of > 9 cm^2.
3. With specified PCB Layout shown in Figure 4 under forced convection airflow condition.
4. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
5. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
   > Go to www.freescale.com
   > Search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx)]
   > Locate your Part Number and in the Details column, select "View"
   > Select "Environmental and Compliance Information"

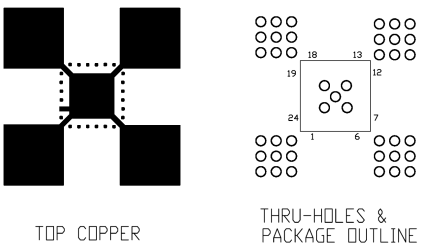


Figure 4. Printed Circuit Board Layout for Maximum Thermal Performance

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 8.0 V ≤ V_{SUP} ≤ 28 V, -0°C ≤ T_A ≤ 85°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range	V+	8.0	12	28	V
Suspend Power Supply Current (6)	I_{SA}	—	2.0	3.0	mA
Operation Power Supply Current (7)	I_Q	—	4.0	6.0	mA
Low V+ Detect Voltage	$V+_{-LV}$	5.0	5.5	6.0	V
Low V+ Detect Hysteresis	V_{LV-HYS}	—	100	—	mV
Logic Inputs Threshold Low (8)	V_{IL}	—	—	0.8	V
Logic Inputs Threshold High (8)	V_{IH}	2.0	—	—	V
Logic Inputs Hysteresis Voltage (8)	V_{I-HYS}	50	300	—	mV
Logic Input Current Low (9)	I_{IL}	—	-50	—	µA
Logic Input Pull-Up Resistance (10)	R_{PULLUP}	—	100	—	kΩ
Hall Inputs Voltage Sensitivity (11)	V_{H-SENS}	50	—	—	mV
Hall Inputs Common Mode Voltage Range (11)	V_{H-CMM}	0.0	—	3.0	V
Hall Inputs Hysteresis Voltage (11)	V_{H-HYS}	—	15	—	mV
Hall Input Current (11)	I_H	-10	—	10	µA
Charge Pump Output Voltage	V_{GHS}	—	—	(V+) +12	V
Charge Pump Reservoir Capacitor	C_{CRES}	—	0.1	—	µF
Charge Pump Capacitor	C_{CP}	—	0.1	—	µF
Logic Output Voltage Low (12)	V_{OL}	—	—	0.4	V
Logic Output Leakage Current High (13)	I_{OH}	—	—	10	µA
Hall Sensors Supply Voltage(14)	V_H	—	—	(V+) -1.0	V

Notes

6. With device in suspend mode (RUN command = False).
7. The current consumed internal to the IC, but not including current output for motor drive.
8. PWM, RUN, and DIR pins.
9. PWM, RUN, and DIR pins with R-pullup = 100 kΩ.
10. Internal Pullup resistance value can vary by 20%.
11. HCA-, HCA+, HBC-, HBC+, HAB-, HAB+ pins.
12. TACH and 3XTACH pins @ I_{OL} = 5.0 mA.
13. TACH and 3XTACH pins @ V_{OH} = 24 V.
14. VH pin @ I_o-hall = 10 mA.

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{SUP} ≤ 28 V, -0°C ≤ T_A ≤ 85°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
High Side R_{DS-ON} (15)	R_{ON-T}	—	0.25	0.5	Ω
Low Side R_{DS-ON} (15)	R_{ON-B}	—	0.25	0.5	Ω
High Side R_{DS-ON} (hot) (16)	R_{ON-T_REF}	—	0.3	0.6	Ω
Low Side R_{DS-ON} (hot) (16)	R_{ON-B_REF}	—	0.3	0.6	Ω
H-bridge MOSFETs' Body-Diode Forward Voltage Drop(17)	V_{F-LD}	—	1.2	—	V
Stall Detection Timer Output Current	I_{O-LDC}	—	128	—	µA
Stall Detection Timer Detection Voltage	$V\text{-}CT_{DET}$	—	2.5	—	V
Current Limit Sense Voltage Threshold	V_{ISENS}	0.09	0.1	0.11	V
Thermal Shutdown Temperature	T_{SD}	150	165	180	°C
T_{SD} Hysteresis	T_{SD-HYS}	—	30	—	°C

Notes

15. @ T_A = 25°C, 14 V =< V+ =< 28 V, I_O = 1.0 A.
16. Typical value (for reference only) @ 85°C =< T_J =< 150°C, 8.0 V =< V+ =< 14 V. Not tested; not guaranteed.
17. @ I_F = 1.0 A for each output MOSFET (measured from source to drain).

DYNAMIC ELECRTICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -0°C ≤ T_A ≤ 85°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Charge Pump Switching Frequency	F_{CP}	—	250	—	kHz
High-Side Gate-Drive Supply Wake-Up Time	T_{WAKE}	—	1.0	2.0	ms
Controlled Braking Period	T_{CBRK}	—	20	—	ms
Low V+ Detect Suspend Time	T_{SPND}	—	100	—	µs
Power-On Reset Wait Time	T_{WAIT}	—	1.0	—	ms
Maximum PWM Input Frequency	F_{PWM}	—	—	100	kHz
Propagation Delay Time (18)	T_{DELAY}	—	—	(1.0)	µs
Output Low Side Off Time (Rise) (18)	T_{LS-OFF}	—	(25)	—	ns
Output High Side On Time (Rise) (18)	T_{HS-ON}	—	(25)	—	ns
Output High Side Off Time (Fall) (18)	T_{HS-OFF}	—	(25)	—	ns
Output Low Side On Time (Fall) (18)	T_{LS-ON}	—	(175)	—	ns
Shoot Through Prevention Time (Output H-bridge High-Z) (18)	T_{OFF}	—	(100)	—	ns

Notes

18. Load condition: Star connected 5.6 Ω load resistances (approximates 1.0 A output current at 12V V+).

TIMING DIAGRAMS

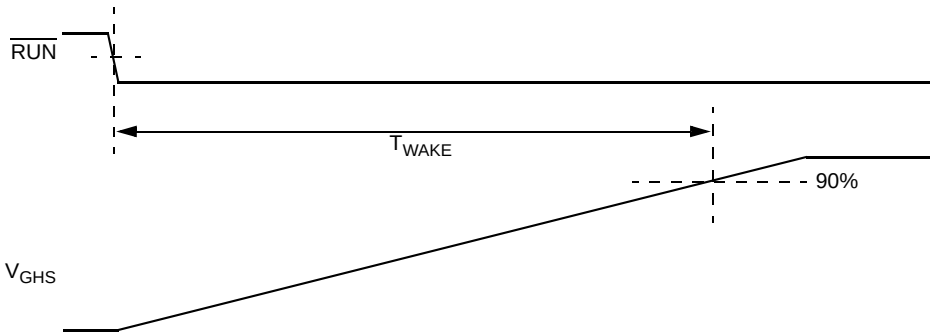


Figure 5. High-Side Gate-Drive Supply Wake-Up Time “Twake”

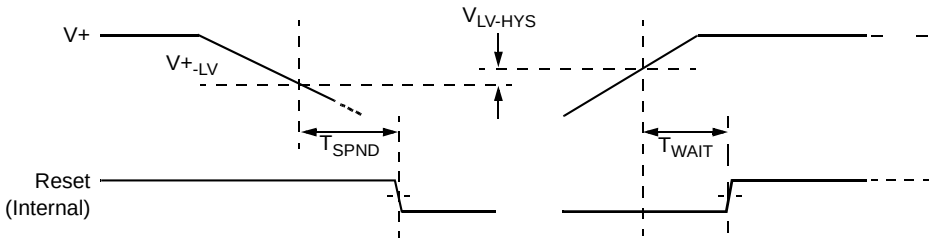


Figure 6. Timing for Reset on Low V+ Detect

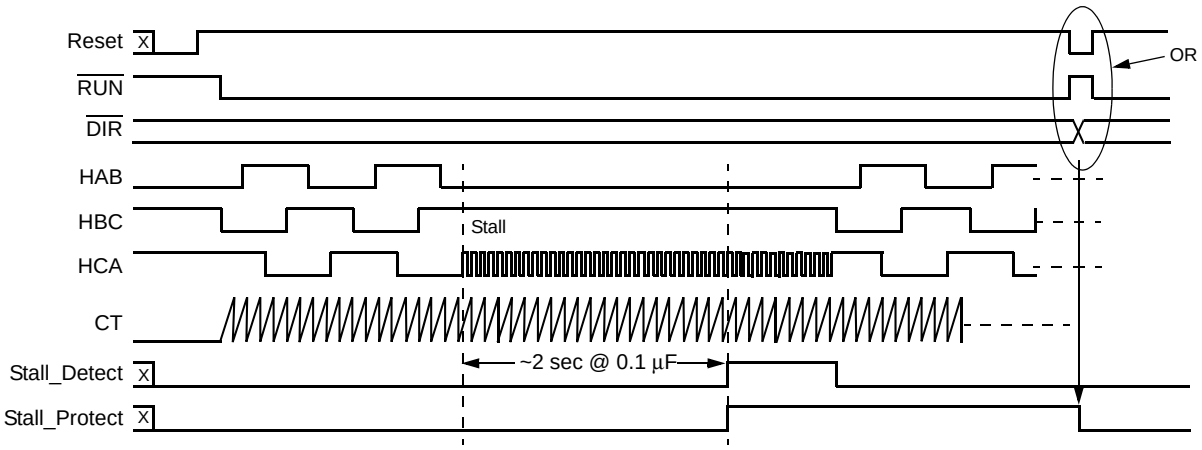


Figure 7. Stall Detection/Protection Timing

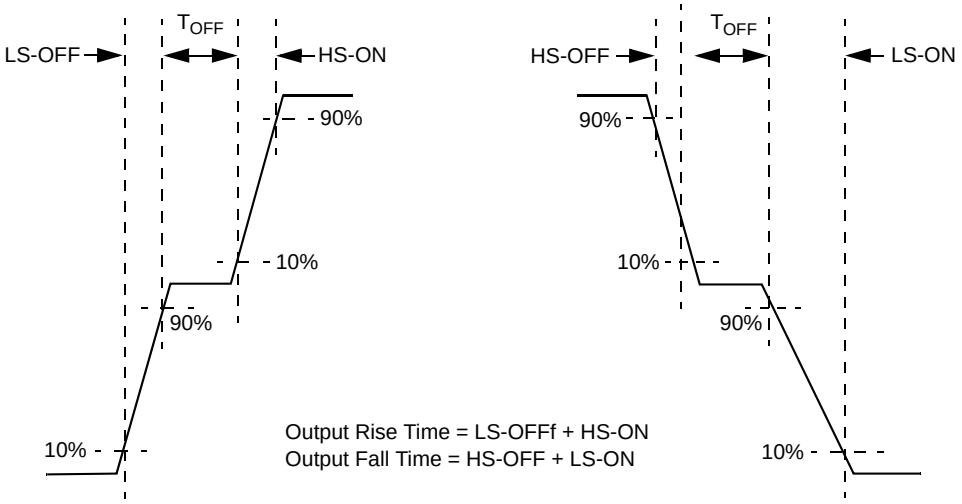


Figure 8. Rise Time, Fall Time, Shoot Through Prevention Timing

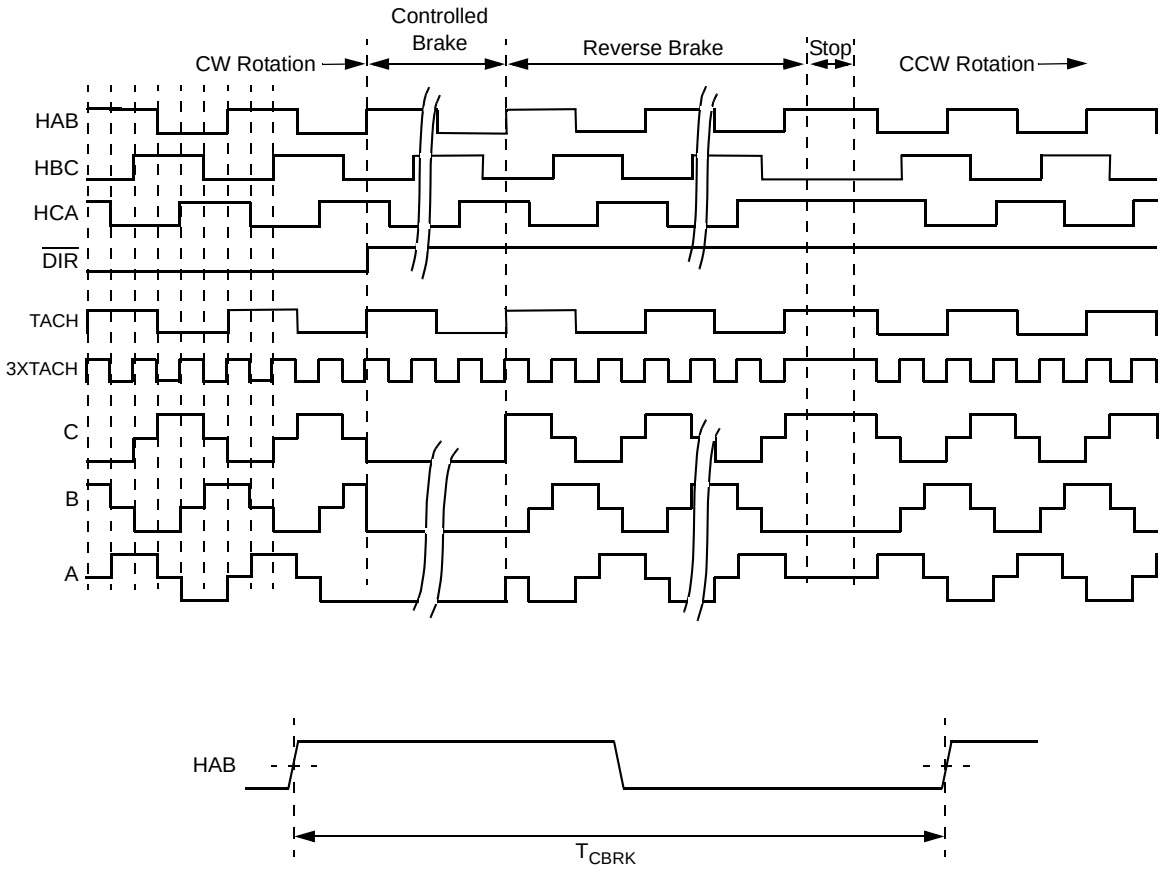


Figure 9. Controlled Brake Mode Timing

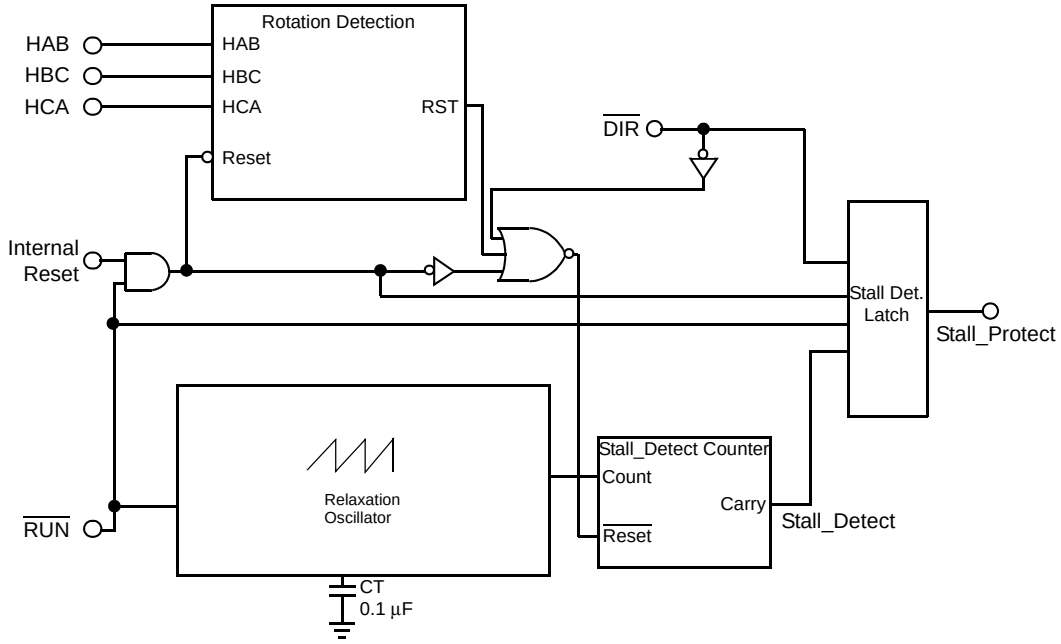


Figure 10. Stalled Rotor Detection Logic Diagram

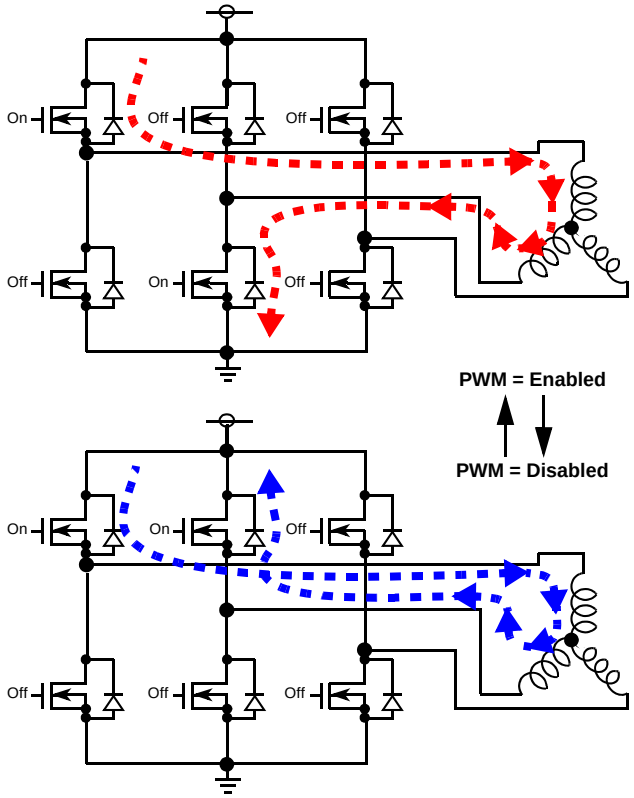


Figure 11. Synchronous Rectification "Slow-Decay Current" Example

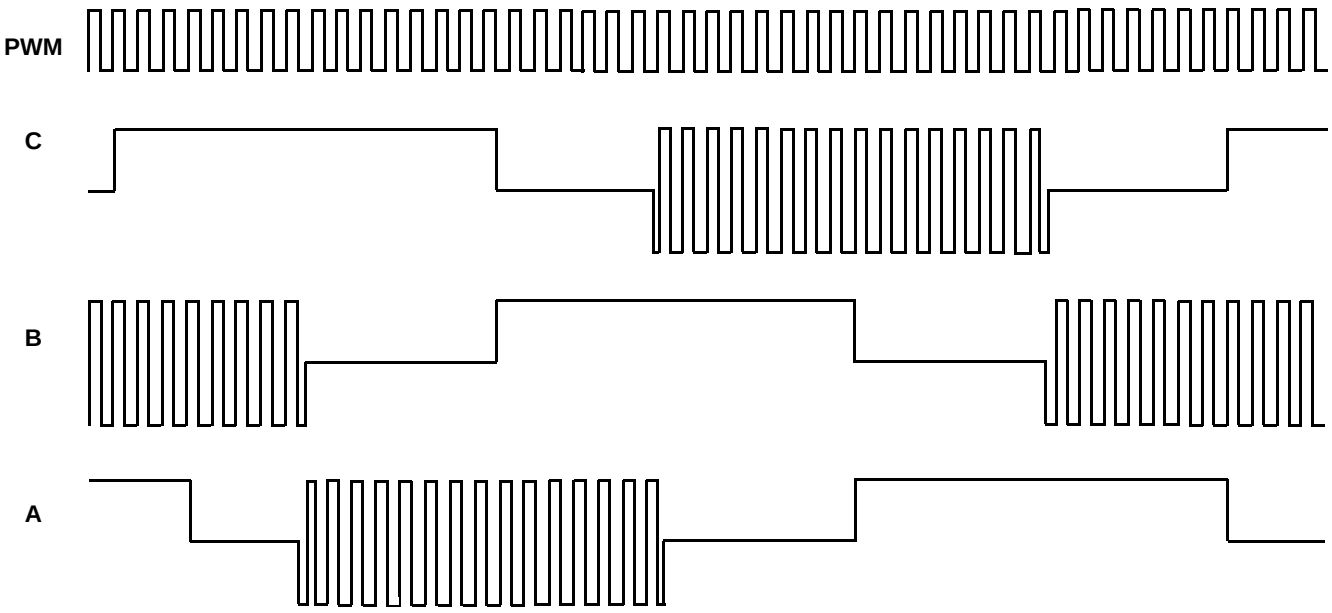


Figure 12. PWM Switching Waveforms

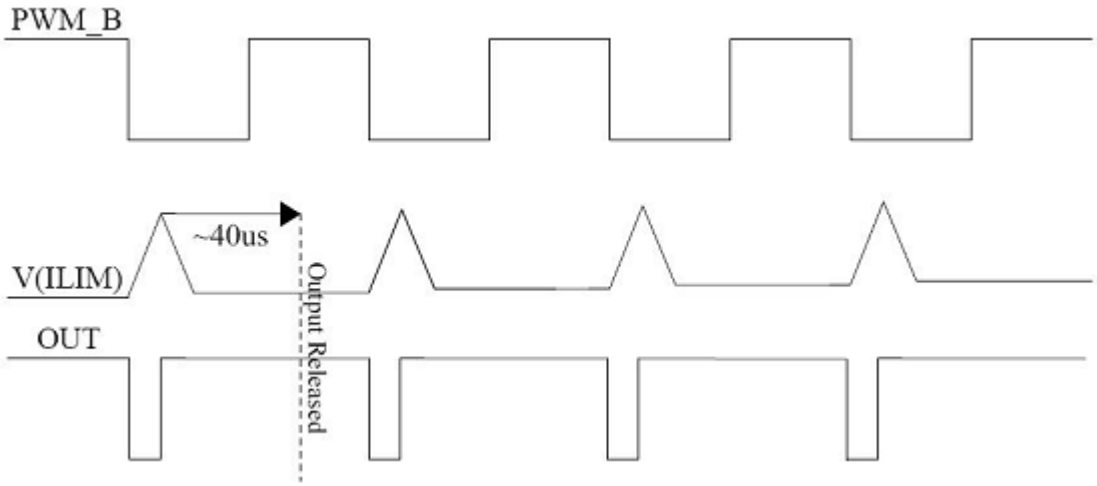


Figure 13. ISENS Current Limit Waveforms

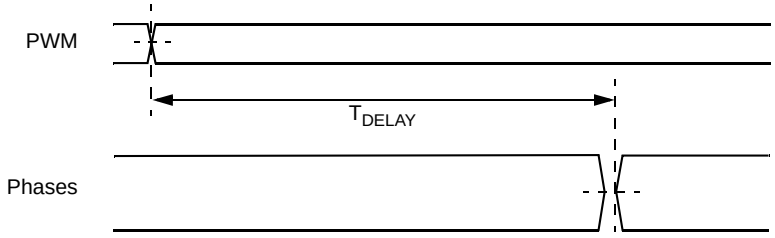


Figure 14. Propagation Delay

FUNCTIONAL DESCRIPTION

INTRODUCTION

The MC34929 Brushless DC Motor Driver IC is a complete BLDC motor driver system in one chip. It is designed to efficiently drive three-phase BLDC motors up to 1.0 A and 28 V, and has built in protection features making it ideal for a variety of consumer and office applications containing small motors. Because it has a built-in Hall-sensors interface and Hall sensors bias supply, it can operate motors either stand-alone (e.g., with pushbutton/switch interface), or under the control of an external MCU. Its sophisticated analog/mixed-signal state machine accommodates several modes of operation, including: clockwise, counterclockwise, run/stop, brake, variable speed (PWM), and torque limit (current limit).

FUNCTIONAL PIN DESCRIPTION

HAL CA NEG (HCA-)

Receives negative output from sensor located between ‘c’ and ‘a’ phases.

HAL CA POS (HCA+)

Receives positive output from sensor located between ‘c’ and ‘a’ phases.

HAL BC NEG (HBC-)

Receives negative output from sensor located between ‘b’ and ‘c’ phases.

HAL BC POS (HBC+)

Receives positive output from sensor located between ‘b’ and ‘c’ phases.

HAL AB NEG (HAB-)

Receives negative output from sensor located between ‘a’ and ‘b’ phases.

HAL AB POS (HAB+)

Receives positive output from sensor located between ‘a’ and ‘b’ phases.

RESERVOIR CAP (CRES)

External charge pump resevoir cap.

CHARGE PUMP POS (CP+)

Positive side of charge pumping cap.

CHARGE PUMP NEG (CP-)

Negative side of charge pumping cap.

POSITIVE SUPPLY (V+)

Main supply input for device and monitor.

SIGNAL GROUND (GND)

Signal ground for the device.

TIMING CAP (CT)

External cap for stall detect timing.

HALL VOLTAGE (VH)

Supply voltage for the external hall sensors.

PHASE C OUTPUT (PHC)

Half bridge output for phase “c” motor winding.

PHASE A OUTPUT (PHC)

Half bridge output for phase “a” motor winding.

LOW SIDE SOURCES (LSS)

Common source pin for lower half of bridge.

PHASE B OUTPUT (PHB)

Half bridge output for phase “b” motor winding.

CURRENT SENSE (ISENS)

Current limiting sense resistor input.

RUN ($\overline{\text{RUN}}$)

Run/stop control input (active low = motor running).

TACH OUTPUT (TACH)

Open-drain-buffered output of sensor ‘ab’.

3X TACH OUTPUT (3XTACH)

Open-drain-buffered, exor’ed output of all three sensors.

DIRECTION ($\overline{\text{DIR}}$)

Direction control input (active low = cw rotation).

POWER GROUND (PGND)

Power ground.

PWM OR ENABLE ($\overline{\text{PWM}}$)

Pwm signal input (active low = outputs enabled).

FUNCTIONAL DEVICE OPERATION

The following paragraphs describe the internal function of the 34929 as shown in Figure 2.

CHARGE PUMP

This charge pump provides the VGHS and internal power supply for the high side power MOSFET gate drive. Its output voltage is limited to V+ +10V to prevent damage to the driver circuits or MOSFET gates. However, VGHS will be below V+ +10V if V+ supply voltage is below 12V. The switching frequency of this charge pump is ~250 kHz. The VGHS supply wakes up typically 1ms after the RUN command is initiated.

REGULATORS AND VOLTAGE REFERENCE

Internal regulators provide operating and reference voltages for use by the analog/mixed-signal circuitry. This function also includes providing the drive voltage for the low-side gate drivers. The regulators for the internal logic and analog circuits comprise regulators for the logic circuits, and regulators for the analog circuits (including input/output buffering, but excepting the power outputs). A bandgap circuit generates the internal precision reference voltage (1.25 V). This is used for biasing the comparators and other analog circuits. (Note: this reference voltage is not externally available.)

INTERNAL CLOCK

The internal clock generates a stable pulse-train for use by the IC's logic circuits. Its output frequency is 1.0 MHz ±30%. The clock circuit also includes frequency-dividers to derive lower frequency pulse trains for use by circuits such as the charge pump and various internal timers, etc.).

INPUT LOGIC

All logic input pins have internal 100K Ω pull-ups connected to the internal Vdd logic supply. The logic input circuitry includes the following inputs:

- **PWM** input controls the speed of motor. Output = "Enable" when PWM = "L", and then Output = "Disable" (means "Z": High Impedance) when PWM = "H".
- **RUN** input controls the start and stop function. When RUN = "H", this IC will go to suspend mode via controlled brake state and suspend unnecessary circuits (Internal OSC, Counters, Charge pump, Stall detection and protection).
- **DIR** input controls the direction of motor. When DIR is flipped, the motor will be reverse, brake through controlled brake, and then rotate to reverse direction. This DIR pin has capability to be applied to V+ + VF.

HALL COMPARATORS

The Hall comparators square-up the signals from the Hall sensors.

HALL SWITCH

A high side switch to turn-on and turn-off the Hall supply current.

TACH, 3XTACH OUTPUT

The TACH outputs are as follows: TACH is the inverted HAB signal. 3XTACH is from inverted EXOR with all three Hall sensor signals. These outputs are both open drain type.

LOW V+ DETECT

The low V+ voltage detection circuit monitors V+; if the V+ voltage falls below the threshold, the IC will reset after T_{SPND} time. This circuitry will not respond to negative-going transients on V+ within the T_{SPND} time period. Once placed in suspend mode, V+ must return to a level greater than the detection threshold plus and additional 100mv (typical) hysteresis, and stay there for the T_{WAIT} period, before the IC will come out of suspend mode.

RESET

The reset function works as follows: when an error condition, such as V+ falling below the $V+_{-LV}$ threshold, is detected, the IC will be in placed in suspend mode (all output MOSFETs set to a high impedance state) by way of a controlled-braking transition state. This will occur regardless of RUN command status. Note, the error condition must exist for a time period greater than T_{SPND} before the internal reset will be generated. When the error condition resolves, suspend mode will be released after the T_{WAIT} period. (See Figure 6.)

STALL DETECTION AND PROTECTION

The stall detection and protection circuit actively monitors operation for a stalled rotor event while the RUN command is set = "True". A stall is detected as follows (see Figure 7):

1) A sawtooth waveform generated at the timing capacitor, TC, is monitored by the stall-detect counter which is counting the sawtooth cycles.

2) The stall-detect counter is being reset (cleared) every time there is a transition on any of the outputs from the Hall comparators (HAB, HBC, or HCA).

3) A "stall condition" is assumed anytime the stall-detect counter is allowed to overflow, (i.e., anytime the counter is not cleared back to zero by the EXOR'ed output of the HAB, HBC, and HCA comparators). This can only occur when at least two of the signals (HAB, HBC, or HCA) have become static (fixed to "H" or "L").

4) Once the internal Stall-Detect signal is asserted, an internal Stall-Protect signal is latched. The Stall-Protect latch keeps the IC in suspend-mode even if the stall condition is subsequently resolved.

5) The Stall-Protect Latch can only be reset by Toggling V+, $\overline{\text{RUN}}$ or $\overline{\text{DIR}}$.

PWM CONTROL

The phase outputs can be controlled with a PWM input. During PWM'ing, the freewheeling currents generated by the motor's windings are synchronously rectified by the output H-bridge to produce a slow decay waveform and avoid dissipating excess power in the IC (see Figure 12).

CURRENT LIMIT

The current limit function provides the means to set the maximum allowed motor current, and thus effectively sets the maximum possible torque the motor can apply to its load. The function is implemented via an external sense resistance R_{ISENSE} through which flows the return current of the 3-phase H-bridge. The voltage drop across R_{ISENSE} is monitored by the ISENS pin, and whenever the threshold of 0.1V is exceeded, the phase that is currently low will be brought high. The output will be released ~40 µs later. The output will then follow the PWM input once again.

CONTROLLED BRAKE MODE

The controlled brake mode prevents high Back-EMF voltages from being created when decelerating the motor to change direction. When the DIR command changes state, all three phases are held low for the time period "T_{CBRK}" (~20 msec @ 500 rpm with a 12-pole rotor). See Figure 12.

SHORT CIRCUIT PROTECTION

The short circuit protection function utilizes sense-FETs in the H-bridge high-side MOSFETs. If a short circuit occurs the sense-FET portion of the affected high-side MOSFET's cells will provide an output to the short-circuit detection circuitry that exceeds the preset threshold, and the short-circuit detection circuitry will immediately set all phase output to LOW (i.e., all low-side MOSFETs will be turned on).

THERMAL SHUTDOWN

The thermal shutdown protection function utilizes an on-chip temperature sensor and a threshold comparator with preset hysteresis. If the die temperature exceeds the T_{SD} temperature threshold, the protection circuitry will immediately set all phase outputs to OFF (i.e., all H-bridge MOSFETs will be set to a high-impedance state). Thermal shutdown reacts to any cause of over-temperature, including that resulting from prolonged running at high currents with insufficient cooling.

LOGIC COMMANDS AND REGISTERS

Table 5. 3 Phase Motor Drive Truth Table

DIR	Hall AB	Hall BC	Hall CA	PWM	C	B	A	TACH	3XTACH
X	L	L	L	X	Z	Z	Z	H	H
X	H	H	H	X	Z	Z	Z	L	L
L	L	L	H	L	Z	H	L	H	H
L	L	H	L	L	H	L	Z	H	H
L	L	H	H	L	H	Z	L	H	L
L	H	L	L	L	L	Z	H	L	H
L	H	L	H	L	L	H	Z	L	L
L	H	H	L	L	Z	L	H	L	L
H	L	L	H	L	Z	L	H	H	H
H	L	H	L	L	L	H	Z	H	H
H	L	H	H	L	L	Z	H	H	L
H	H	L	L	L	H	Z	L	L	H
H	H	L	H	L	H	L	Z	L	L
H	H	H	L	L	Z	H	L	L	L
L	L	L	H	H	Z	H	H	H	H
L	L	H	L	H	H	H	Z	H	H
L	L	H	H	H	H	Z	H	H	L
L	H	L	L	H	H	Z	H	L	H
L	H	L	H	H	H	H	Z	L	L
L	H	H	L	H	Z	H	H	L	L
H	L	L	H	H	Z	H	H	H	H
H	L	H	L	H	H	H	Z	H	H
H	L	H	H	H	H	Z	H	H	L
H	H	L	L	H	H	Z	H	L	H
H	H	L	H	H	H	H	Z	L	L
H	H	H	L	H	Z	H	H	L	L

Notes

DIR: L = CW, H = CCW; Hall Signals: L = (Hx + < Hx-), H = (Hx + > Hx-); PWM: L = Enable, H = Disable

RUN = L, Internal Reset = H, All protections = “L” (Negated).

When PWM is Disabled (H), the output will be in slow decay mode on the high-side with Synchronous Rectification.

Table 6. Suspend Mode and Protection Modes Truth Table

RUN	DIR	Under Voltage	Stall Detect	Current Limit	Short Circuit	TSD	Reset	Stall Protect	PHASES	TACH 3XTACH	HB
SUSPEND MODE											
H	X	X	X	X	X	X	X	X	L->Z	H	Off
THERMAL SHUTDOWN											
L	X	X	X	X	X	H	X	X	Z	H	Off
SHORT CIRCUIT PROTECTION											
L	X	X	X	X	H	L	H	X	L	H	Off
CURRENT LIMIT DETECTION											
L	X	X	X	H	L	L	H	X	Int.PWM	Run	On
STALL DETECTION AND PROTECTION											
L	X	L	H	L	L	L	H	H	Z	Stall	On
L	X	L	L	L	L	L	H	H	Z	Run	On
H->L	X	L	L	L	L	L	H	L	Run	Run	On
L	Flip	L	L	L	L	L	H	L	Run	Run	On
L	X	H->L	L	L	L	L	H	L	Run	Run	On
UNDER VOLTAGE DETECTION											
X	X	H	X	X	X	X	L	L	L->Z	H	Off
L	X	H->L	L	L	L	L	H	L	Run	Run	On
NORMAL MODE											
L	X	L	L	L	L	L	H	L	Run	Run	On

Notes

RUN: Start at “L” and Stop at “H”. “H->L” indicates input is toggled.

DIR: CW direction at “L” and CCW direction at “H” and “Flip” indicates change of logic level to opposite state.

“Under Voltage”, “Stall Detect”, “Current LImit”, Short Circuit”, “TSD”, and “Stall Protect” are “High” active internal signals. “Reset” is a “Low” active internal signal.

Under Voltage: H->L indicates removing then re-applying power (V+).

“Run” status indicates operation in 3-phase commutation mode.

Commanding a “Stop” state from a “Run” state will always result in a transition through the “Controlled Brake” state (to prevent high voltage Back-EMF), before changing to OFF (high-Z).

TYPICAL APPLICATIONS

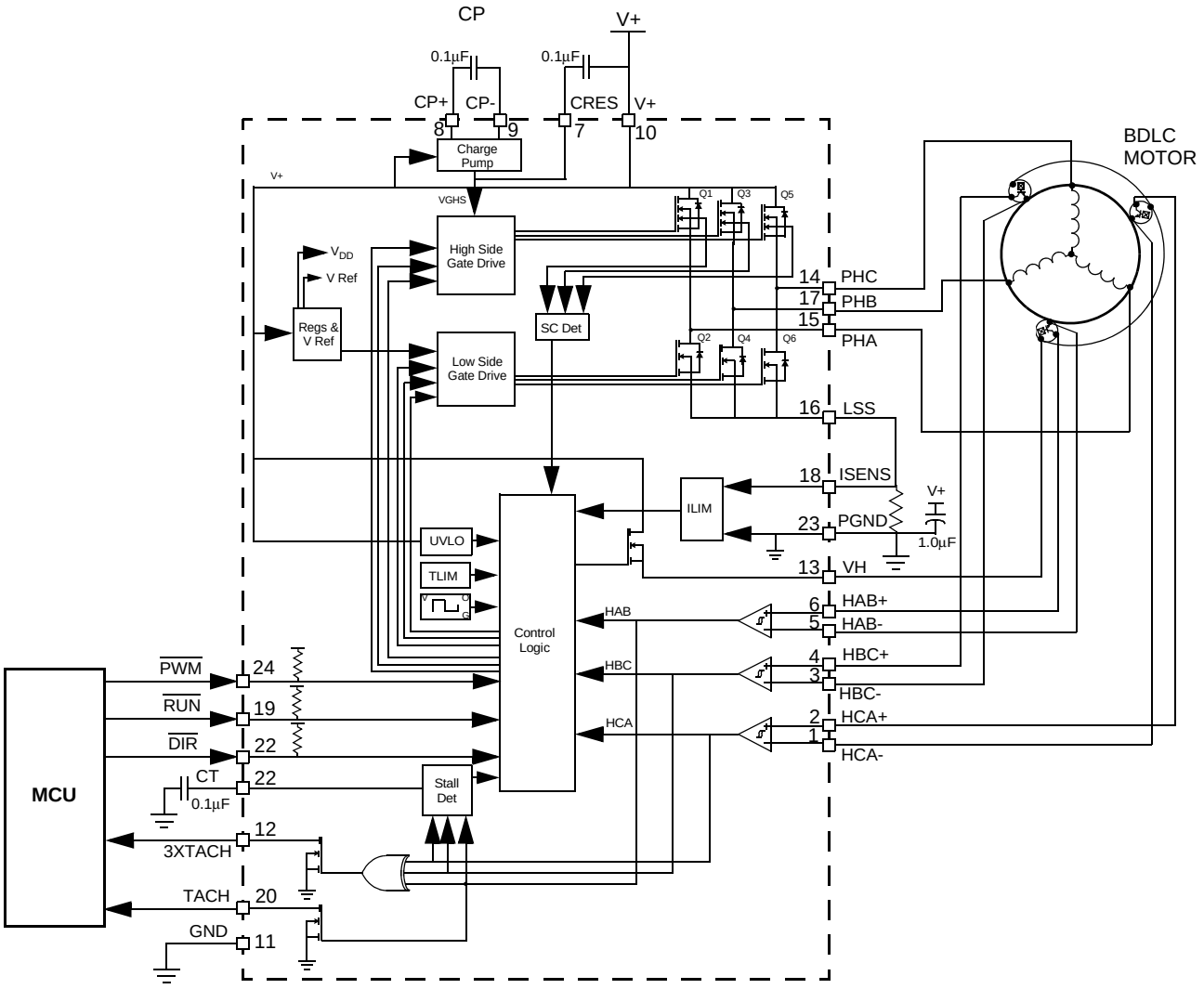
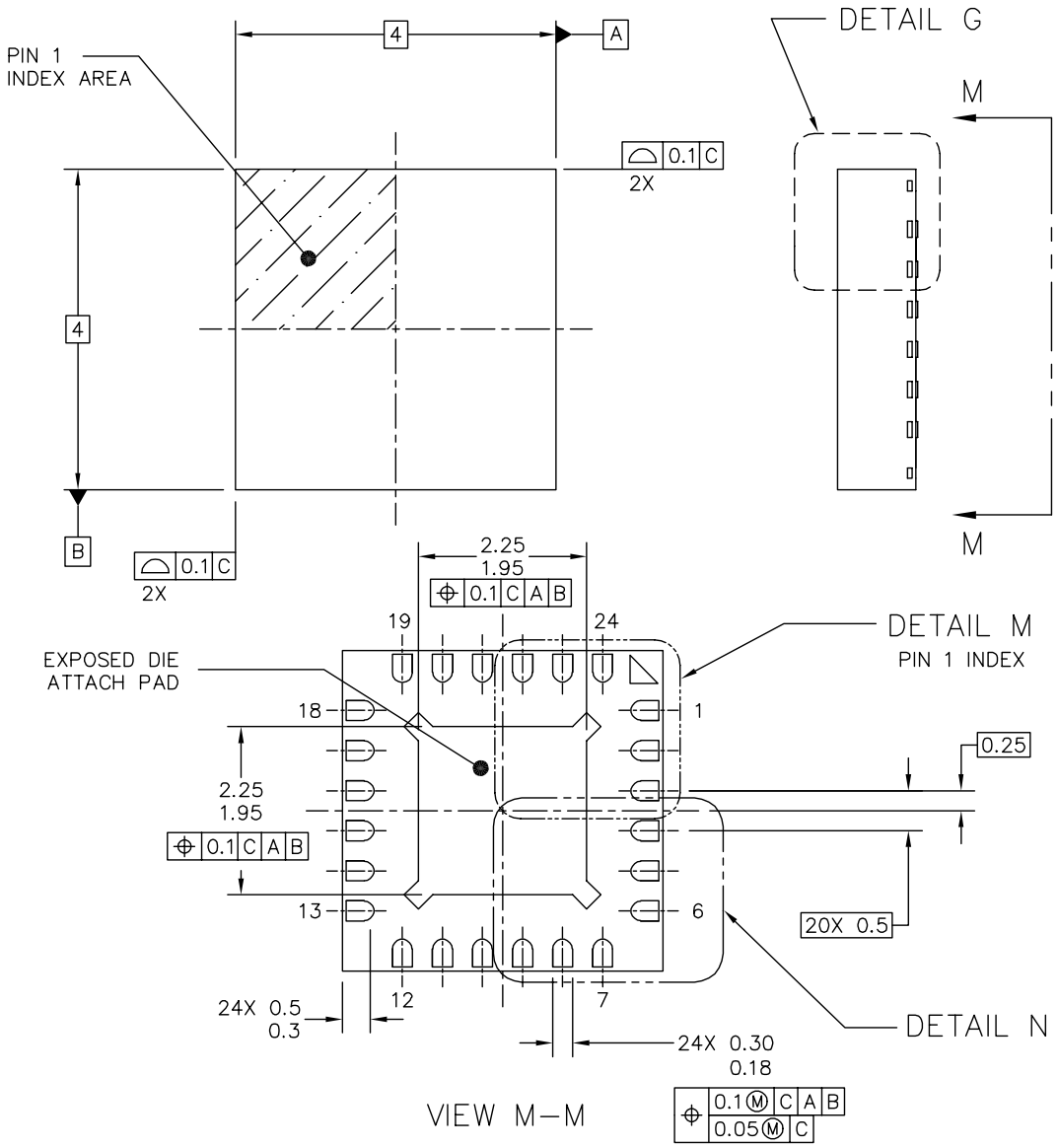


Figure 15. Simple Application Circuit

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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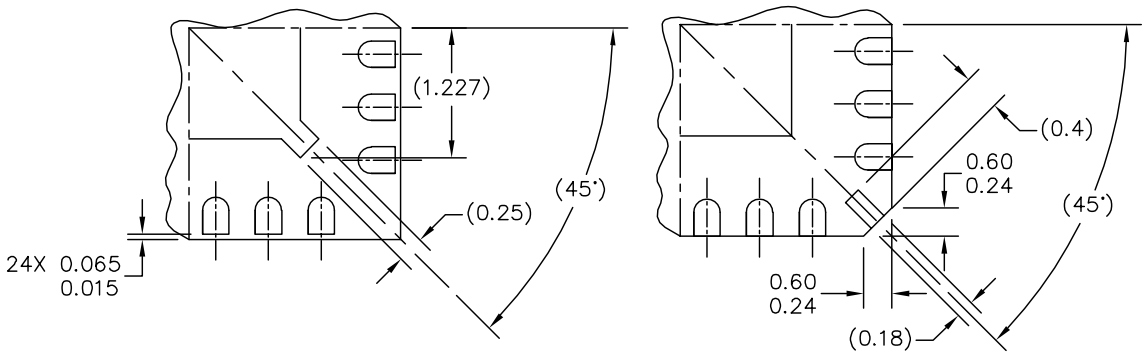
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.5 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ARH99033A	REV: C
	CASE NUMBER: 1307–01	06 SEP 2005
	STANDARD: JEDEC MO–220 VGGD–2	

QFN SUFFIX
24-PIN
PLASTIC PACKAGE
98ARH99033A
ISSUE C

34929

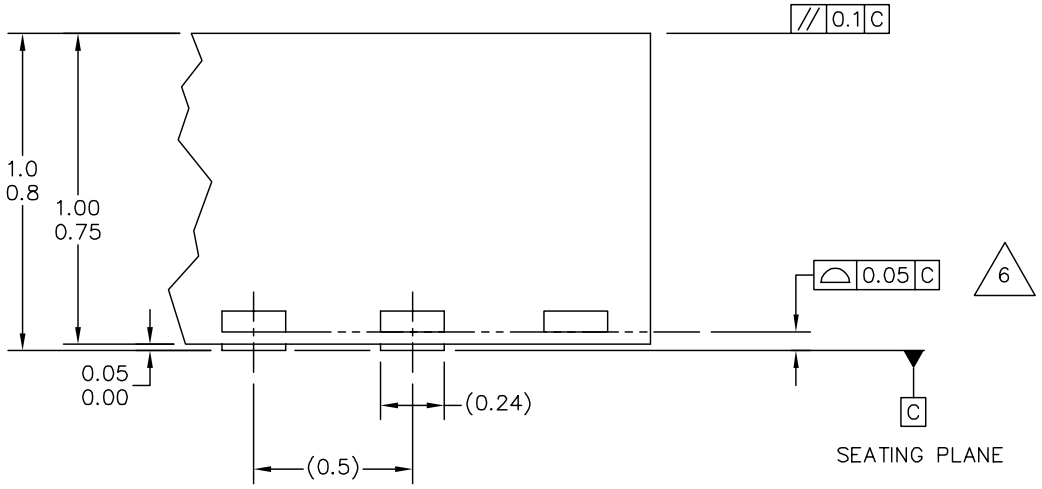


DETAIL N
PREFERRED CORNER CONFIGURATION

4

DETAIL N
CORNER CONFIGURATION OPTION

4 5



DETAIL G
VIEW ROTATED 90° CW

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
6.0	7/2005	• Implemented Revision History page • Updated to the Freescale format • Changed status to Advance

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